EFFICIENT POWER CONVERSION

GaN in Space

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1.0 Why GaN in Space?

Gallium nitride power device technology enables a new generation of power converters for operation in harsh radiation conditions of space. GaN devices operate at higher frequencies, higher efficiencies, and greater power densities than ever achievable before. These power devices can exhibit superior radiation tolerance compared with silicon MOSFETs depending upon specific device design.

This eBook discusses the capabilities of GaN devices that have been specifically designed for critical applications in high reliability or commercial satellite space environments. Some of the failure mechanisms in GaN, and how they impact radiation performance, are explored. The electrical performance of radiation hard GaN transistors is compared with the most popular radiation-hardened (rad-hard) MOSFETs in the market, and examples of motor drives and DC-DC converters are discussed.

GaN-based integrated circuits offer an extraordinary opportunity for improving performance, size, and radiation resistance compared with silicon alternatives. Much like in commercial applications, combining multiple power devices on a single chip with drivers, level-shifting circuits, and protection circuits can enable performance otherwise unobtainable.

A comprehensive analysis of GaN-based solutions, reliability, and applications are available in EPC's latest text book, ***GaN Power Devices and Applications***, released in October, 2021. The book is available for purchase on **EPC's web site**.

1.1 Radiation Effects in GaN

There are three primary types of radiation experienced by semiconductors used in space applications. Regardless of whether devices are being employed in satellites orbiting around our earth or incorporated in exploration satellites visiting the most distant parts of our solar system, all semiconductors experience some form of high-energy radiation bombardment. These types of radiation are gamma radiation, neutron radiation, and heavy ion bombardment.

An energetic particle can cause damage to a semiconductor in fundamentally three ways; it can cause traps in non-conducting layers, it can cause physical damage to the crystal or insulator, also called displacement damage, or the particle can generate a cloud of electron-hole pairs that will cause the device to momentarily conduct, and possibly burn out in the process [1].

In GaN devices, energetic particles cannot generate momentary short-circuit conditions because mobile hole-electron pairs cannot be generated. Thus, this chapter will focus on the first two failure mechanisms – trapping and physical damage.

1.1.1 Gamma Radiation – Trapping in Silicon MOSFETs

Gamma radiation consists of high energy photons that interact with electrons. Figure 1.1 (a) is a cross section of a typical silicon MOSFET. It is a vertical device with the source and gate on the top surface and the drain on the bottom surface. The gate electrode is separated from the channel region by a thin silicon dioxide layer.

In a silicon based MOSFET, the gamma radiation knocks an electron out of the silicon dioxide layer leaving behind a positively charged 'trap' in the gate oxide [1, 2]. The positive charge reduces the threshold voltage of the device until the transistor goes from normally off – or enhancement mode – to normally on, which is a depletion-mode state. At this point the system will need a negative voltage to turn the MOSFET off. Typical ratings for rad-hard devices range from 100 kRads to 300 kRads. In some cases, devices can be made to go up to 1 MRad, but these tend to be very expensive.

1.1.2 Gamma Radiation – Enhancement-Mode GaN Transistors

Enhancement-mode GaN devices are built very differently from silicon MOSFETs. As shown in Figure 1.1 (b), all three terminals; gate, source, and drain, are located on the top surface. As in a silicon MOSFET, conduction between source and drain is modulated by biasing the gate electrode from zero volts to a positive voltage – usually 5 V. In enhancement-mode GaN devices the gate is separated from the underlying channel by an aluminum gallium nitride layer. This layer does not accumulate charge when subjected to gamma radiation.

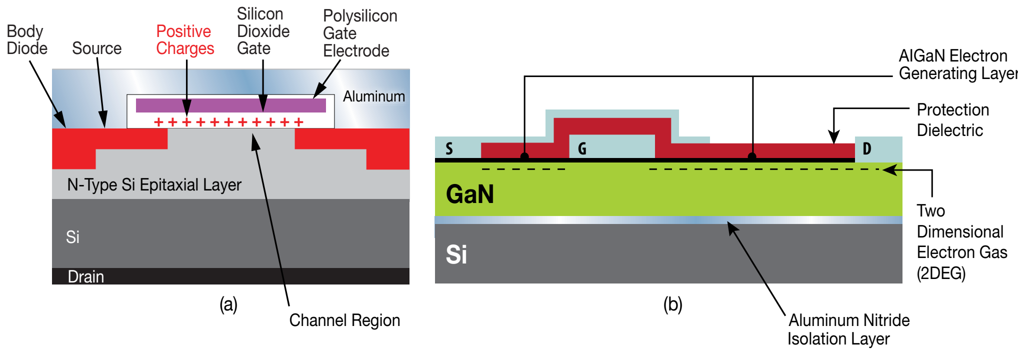
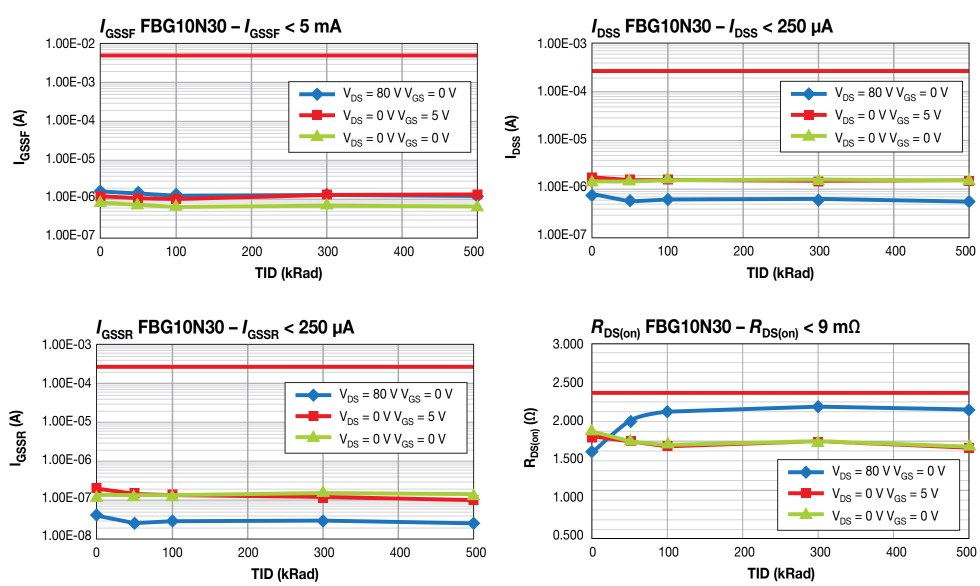


Figure 1.1 (a) Cross section of a typical silicon MOSFET (b) Cross section of a typical enhancement-mode

As an example of the performance of rad-hard GaN devices, 100 V GaN-on-Si transistors were subjected to 500 kRad of gamma radiation. Throughout the testing, leakage currents from drain to source and gate to source, as well as the threshold voltage and on-resistance of the devices at various checkpoints along the way were measured, to confirm that there are no significant changes in device performance. Since the initial testing, these same GaN devices have been subjected to 50 MRads, confirming that enhancement-mode GaN devices built as in shown in Figure 1.1 (b) will not be the first part in any space system to fail due to gamma radiation. Testing results are shown in Figure 1.2. Additional testing and analysis can be found in reference [3].



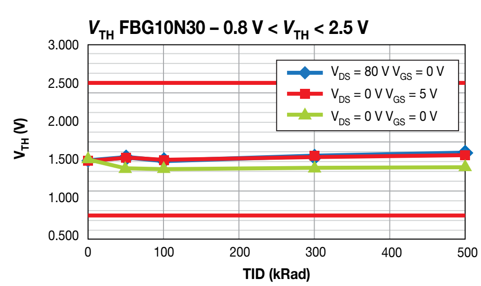


Figure 1.2 Results of gamma radiation testing of eGaN devices to 500 kRads

1.1.3 Neutron Radiation

The primary failure mechanism for devices under neutron bombardment is displacement damage [4]. High energy neutrons will scatter off atoms in the crystal lattice and leave behind lattice defects. Figure 1.3 shows the impact of neutron radiation at doses up to 1 x 10^{15} per square cm. As with gamma radiation, the impact of neutrons on the GaN crystal and the entire device structure is minimal.

The reason for GaN's superior performance under neutron radiation is that GaN has a much higher displacement threshold energy compared with silicon. The displacement energy of a crystal is proportional to the bond strength of the crystalline elements. The bond energy between gallium and nitrogen is significantly higher than the bond energy between silicon atoms in a silicon power MOSFET as shown in Figure 1.4 [5].

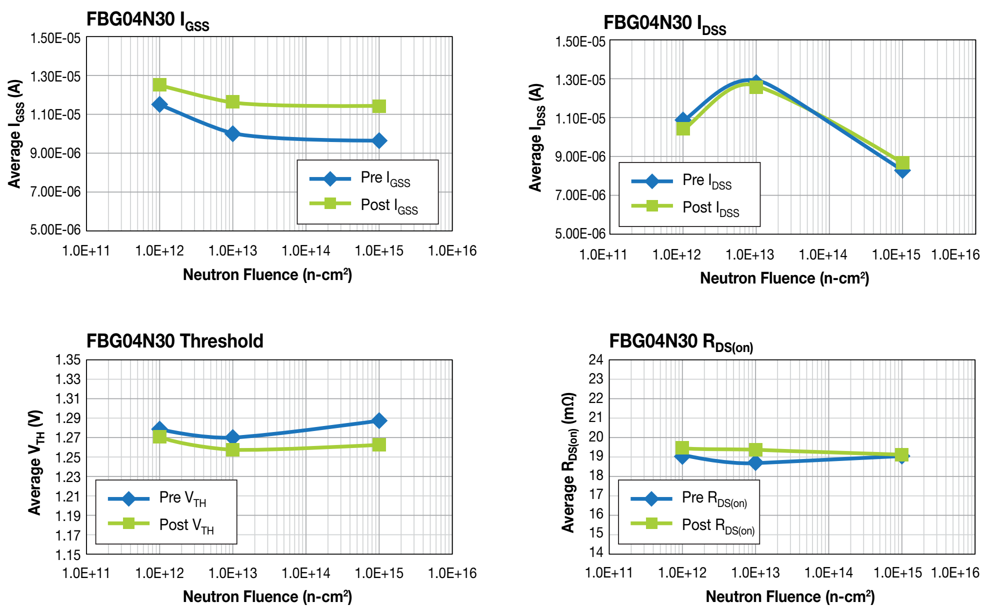


Figure 1.3 Impact of neutron radiation on eGaN devices at doses up to 1 x 10^{15} per square cm

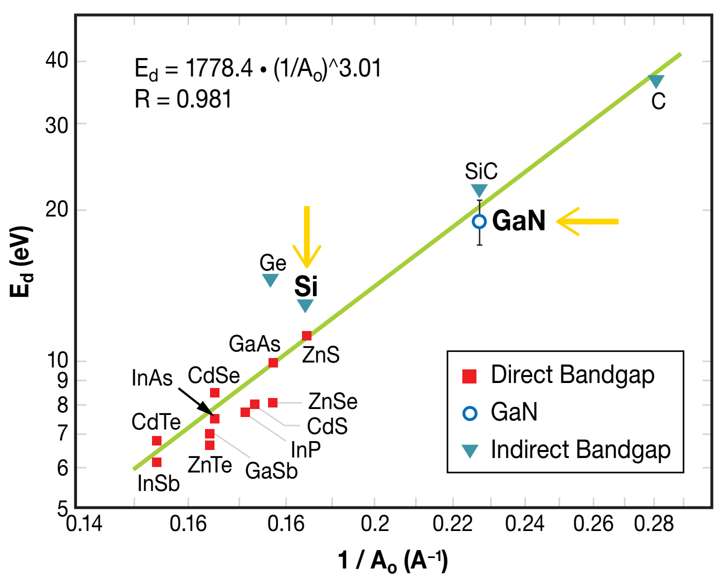


Figure 1.4 Graph of displacement threshold energy versus the inverse of the lattice constant for different materials taken from [5]

1.1.4 Single Event Effects (SEE) – Si MOSFETs

SEE are caused by heavy ions generated by the impact of galactic cosmic rays, solar particles or energetic neutrons and protons. This terrestrial condition can be simulated by using a cyclotron to create beams of different ions. Two of the most common ions used to evaluate radiation tolerance of electronics components are xenon, with a linear energy transfer (LET) at about 50 MeV·cm^2/mg, and gold, with an LET at about 85 MeV·cm^2/mg.

In a silicon MOSFET there are two primary failure mechanisms caused by these heavy ions, single event gate rupture (SEGR) and single event burnout (SEB). SEGR is caused by the energetic atom creating such a high transient electric field across the gate oxide that the gate oxide ruptures, as illustrated in the upper cross section in Figure 1.5. Whereas SEB is caused when the energetic particle transverses the drift region of the device where there are relatively high electric fields. The energetic particle loses its energy while generating a large number of hole electron pairs.

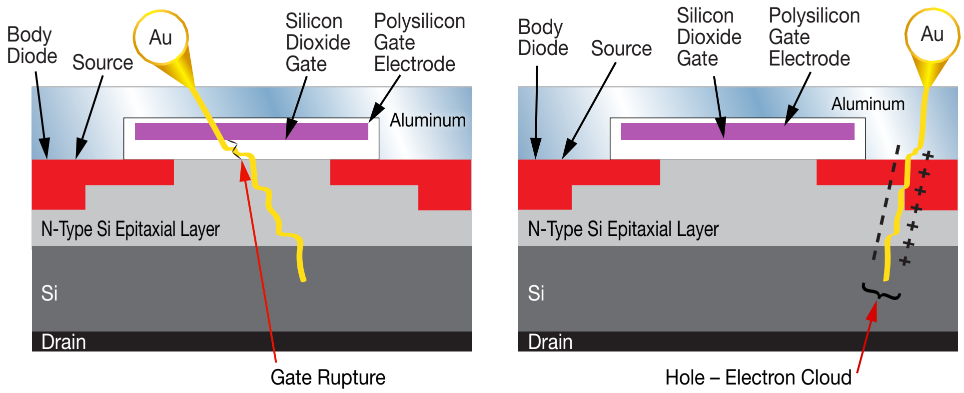


Figure 1.5 (Top) In Si MOSFETs heavy ions impacting gate regions can cause ruptures in the thin gate oxide region. This phenomenon is called Single Event Gate Rupture (SEGR). (bottom) Heavy ions penetrating drain and source regions can cause clouds of hole-electron pairs to be generated that appear as a momentary short circuit. This phenomenon is called Single Event Upset (SEU).

These hole electron pairs crossing the drift region cause the device to momentarily short circuit between drain and source, as shown in the bottom cross section in Figure 1.5. This short circuit can either destroy the device, which is a single event burnout, or the device can survive, appearing as a momentary short circuit that can cause damage to other components in the system. This latter case is call single event upset (SEU).

1.1.5 Single Event – GaN Devices

Since enhancement-mode GaN devices built, as in Figure 1.1 (b), do not have a gate oxide, they are not prone to single event gate rupture. Also, since eGaN devices do not have the ability to conduct large numbers of holes very efficiently, they are not prone to single event upset.

The primary failure mechanism for enhancement-mode GaN devices under heavy ion bombardment is caused by energetic particles crossing the drift region of the device where there are relatively high electric fields. The conditions are about the maximum conditions possible, with a LET beam at 85 MeV·cm^2/mg of gold atoms of gold atoms pummeling the device biased at the maximum data sheet limit. As shown in Figure 1.6, in testing, the gate leakage does not go up during bombardment. The drain-source leakage, however, does start to rise as the displacement damage from the heavy ions increases. For more research on GaN device SEE performance, see references [6–10].

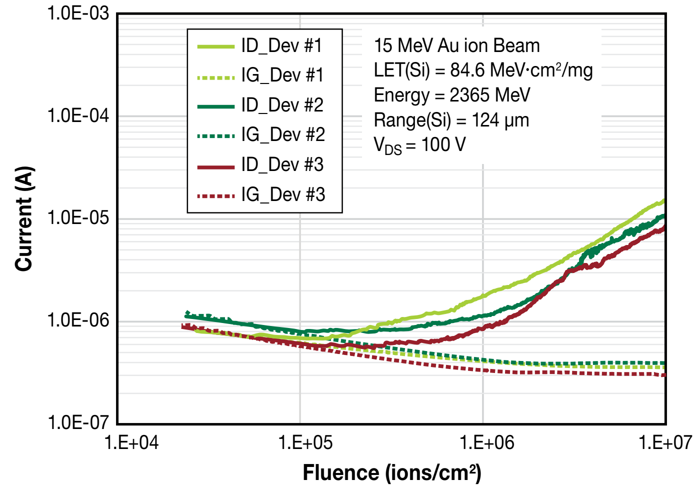


Figure 1.6 I_{DSS} and I_{GSS} progression for FBG10N30 GaN transistor during single event testing up to a fluence of 1 x 10^7 ions/cm^2 AU at a LET level at 84.6 MeV·cm^2/mg and biased at 100 V_{DS}

1.1.6 SEE Safe Operating Areas

Many specially produced enhancement-mode GaN transistors have been tested for SEE under varied conditions – 40 V and 100 V product did not fail under any conditions up to full rated voltage and at a LET level at 87 MeV·cm^2/mg. Figure 1.7 shows the results for several commercially available FBG20N18 200 V products and FBG30N04 300 V products from EPC Space. For the 200 V products, the first failures occurred at a LET level at 85 MeV·cm^2/mg and 190 V, as shown in the red circle on the left. The FBG30N04 300 V product failed at a LET level at 85 MeV·cm^2/mg and 310 V, as shown in the red circle on the right.

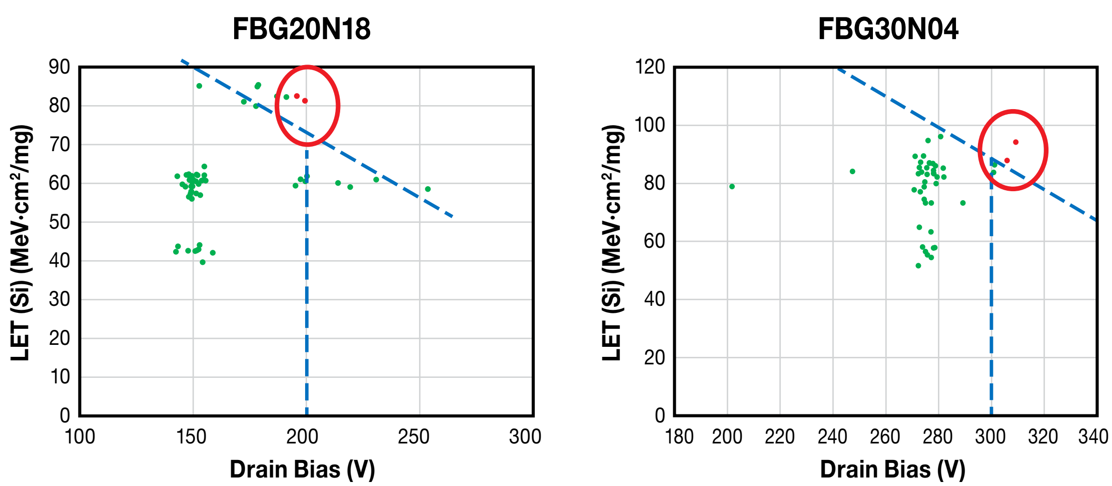


Figure 1.7 Results from several FBG20N18 200 V products (left) and FBG30N04 300 V products (right)

1.1.7 Electrical Performance Comparison

In addition to the superior rad-hard advantages of gallium nitride over silicon, GaN has superior electrical performance. As an example, the electrical performance comparisons of 60 V, 100 V, and 200 V rad-hard GaN transistors against rad-hard power MOSFETs are shown in Table 1.1.

The 60 V EPC7014 and the 100 V FBG10N30 packaged part have half the on-resistance compared to the silicon MOSFET yet are each is one-tenth the size and have about one-twentieth the gate and gate-drain charges that determine switching speed then their comparable MOSFET devices. In addition, the radiation resistance is significantly higher for these two GaN devices.

At 200 V, the difference in electrical performance of the GaN transistors is even greater. Note that the GaN device listed on the left side of the 200 V section of Table 1.1 has similar on-resistance to its MOSFET counterpart, yet is one-tenth the size, and has about 30 times better switching performance while demonstrating superior radiation resistance.

Table 1.1 Electrical performance comparisons rad-hard GaN transistors from EPC Space against power MOSFETs from Infineon

60 V

Parameter	EPC7014	IRHLUB770Z4/ JANSR2N7616UB	IRHLUB730Z4/ JANSF2N7616UB
V_{DS}	60 V	60 V	60 V
I_D	2.4 A	0.8 A	0.8 A
$I_{D\ pulsed}$	4 A	3.2 A	3.2 A
$R_{DS(on)}$	340 mΩ	680 mΩ	680 mΩ
$Q_{G\ max}$	0.2 nC	3.6 nC	3.6 nC
Q_{GD}	0.03 nC	1.8 nC	1.8 nC
Radiation level	1 MRad	100 kRads	300 kRads
SEE LET (MeV·cm^2/mg)	85	85	85
Size	0.8 mm^2	9 mm^2	9 mm^2

100 V

Parameter	FBG10N30	IRHNA67160	Units
I_D	30	35	A
I_{DM}	120	140	A
BV_{DSS}	100	100	V
$R_{DS(on)}$	9	18	mΩ
Q_G	9	160	nC
Q_{GD}	2	65	nC
Q_{RR}	0	1.9	µC
$R_{\theta JC}$	2.12	0.5	°C/W
Radiation Level	> 10 M	300 k	Rad (Si)
SEE (LET level at 85 MeV·cm^2/mg))	100	100	V
Size	23	236	mm^2

Parameter	FBG10N05	IRHNJ67130	Units
I_D	5	22	A
I_{DM}	40	88	A
BV_{DSS}	100	100	V
$R_{DS(on)}$	38	42	mΩ
Q_G	2.2	50	nC
Q_{GD}	0.6	20	nC
Q_{RR}	0	3	µC
$R_{\theta JC}$	3.6	1.67	°C/W
Radiation Level	> 10 M	300 k	Rad (Si)
SEE (LET level at 85 MeV·cm^2/mg))	100	100	V
Size	12	78.5	mm^2

200 V

Parameter	FBG20N18	IRHNA67260	Units
I_D	18	56	A
I_{DM}	72	224	A
BV_{DSS}	200	200	V
$R_{DS(on)}$	26	28	mΩ
Q_G	6	240	nC
Q_{GD}	1.95	60	nC
Q_{RR}	0	11.7	µC
$R_{\theta JC}$	2.12	0.5	°C/W
Radiation Level	> 10 M	300 k	Rad (Si)
SEE (LET level at 85 MeV·cm^2/mg))	175	170	V
Size	23	236	mm^2

Parameter	FBG20N18	IRHNJ67230	Units
I_D	18	16	A
I_{DM}	72	64	A
BV_{DSS}	200	200	V
$R_{DS(on)}$	26	130	mΩ
Q_G	6	50	nC
Q_{GD}	1.95	20	nC
Q_{RR}	0	3.5	µC
$R_{\theta JC}$	2.12	1.67	°C/W
Radiation Level	> 10 M	300 k	Rad (Si)
SEE (LET level at 85 MeV·cm^2/mg))	175	170	V
Size	23	78.5	mm^2

GaN power transistors and ICs are the best choice for power conversion applications in spaceborne systems. Enhancement-mode GaN devices have proven to be more rugged than rad-hard MOSFETs when exposed to various forms of radiation. In addition, the electrical performance of GaN devices is many times superior to the aging silicon power MOSFET. The next section will analyze the specific benefits of GaN devices in a key DC-DC application in satellite power systems. The subsequent section will look at motor drives.

1.2 GaN Transistors for DC-DC Space Designs

Power electronics engineers are constantly working toward designs with higher efficiency and higher power density, while maintaining high reliability and minimizing cost. Advances in design techniques and improved component technologies enable engineers to consistently achieve these goals. Power semiconductors are at the heart of these designs and their improvements are vital to better overall system performance. In this section how GaN power semiconductors allow for innovation in the harsh radiation environments of space applications will be demonstrated.

GaN power semiconductors offer high reliability power system designers a sudden and significant improvement in electrical performance over their silicon power MOSFET predecessors. Table 1.2 compares radiation-hardened GaN and Si power semiconductor device characteristics important for circuit designers to increase efficiency and power density in their converter.

While the comparisons in Table 1.2 show the benefits of a new power semiconductor technology, it can be hard to estimate how these improvements with GaN devices will translate into real world circuit performance where the power semiconductor is part of a larger system. The theoretical impact of these device characteristics on converter performance using the power semiconductor commutation diagram in Figure 1.8 will be explained and the impacts on an innovative real-world product design using the VPT SGRB10028S [11] DC-DC converter, shown in Figure 1.9, will be described.

Table 1.2 Comparison of radiation-hardened GaN and Si MOSFET power semiconductor device characteristics

Device characteristic	200 V GaN (EPC Space FBG20N18B)	200 V Si MOSFET (Infineon IRHNA67260)	Technology comparison
V_{DS} (V)	200	200	Same
$R_{DS(on)}$ (mΩ)	26	28	Similar
Device area (mm^2)	23	237	10 x reduction
Q_G (nC)	6	240	40 x reduction
Q_{GD} (nC)	2	60	30 x reduction
Q_{GS} (nC)	2	70	35 x reduction
C_{OSS} (pF) at 50 V V_{DS}	300	900	3 x reduction
C_{OSS} (pF) at 1 V V_{DS}	950	10000	10 x reduction
Q_{RR} (nC)	0	11700	Infinite reduction
V_{DS} (V)	1.75	1.2	1.5 x increase

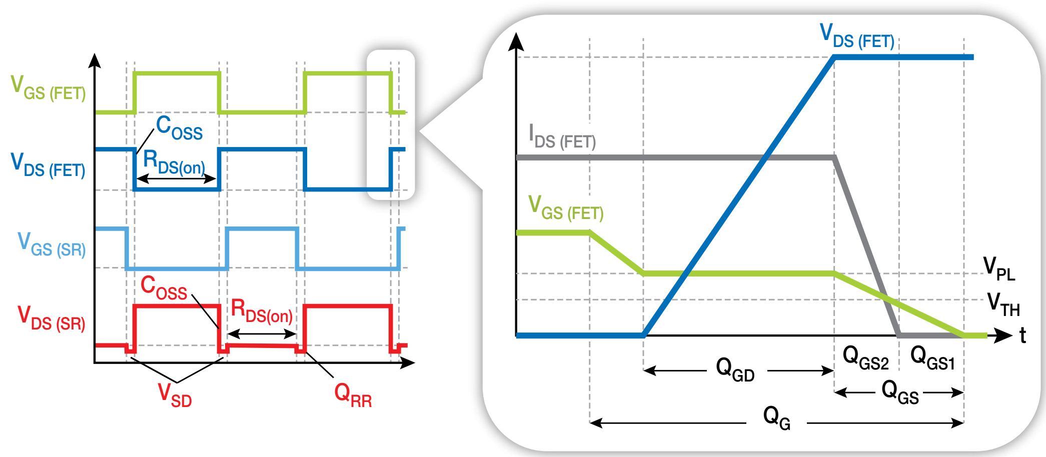


Figure 1.8 Ideal waveforms and loss mechanisms for a hard-switched synchronous power converter

The SGRB10028S has a 100 V input, an adjustable single output from 12 V to 28 V, output power up to 400 W, and efficiencies above 96%. The SGRB converter employs a phase-shifted full-bridge circuit topology with GaN devices used for both the primary devices and the secondary synchronous rectifiers.

Referring to the first entry in Table 1.2, V_{DS}, which is the maximum drain-to-source blocking voltage of the power semiconductor, must be large enough to support the off-state drain-to-source voltage shown in Figure 1.8. This blocking voltage must also have adequate margin, which includes circuit voltage ringing, introduced mainly by parasitic inductances in the circuit. Most of the blocking voltage is dependent on the isolation transformer leakage inductance spike and the design input and output voltages. Thus, for GaN and Si designs, the voltage stresses, and therefore maximum drain-to-source blocking voltage, will be the same.

Device on-state drain-to-source resistance ($R_{DS(on)}$), determines conduction losses. In this design example, a high current is required to reach the high-power demands and the lowest on-resistance devices available were selected, which are similar between GaN and Si power semiconductors at 26 mΩ and 28 mΩ, respectively.

While the on-resistance of these two power semiconductors is similar, the device area and PCB space required by each are very different. The GaN power semiconductor is about one-tenth of the size of the Si MOSFET. In this design, shown in Figure 1.8, the GaN power semiconductor occupies roughly 5-10% of the board space on one side of the design; if the designer had to use a 10 times larger Si MOSFET, the board space occupied would jump to over 50%. This would greatly impact the design of the other components, in particular the magnetics, forcing them to become smaller and limiting the use of integrated magnetics, both of which increase losses and degrade converter efficiency. Advantages like this do not show up in Table 1.2 and Figure 1.8 but have a major impact on system performance.

As the device size shrinks, the losses must be reduced proportionally to avoid becoming a thermal bottleneck in the design. The remainder of Table 1.2 relates to switching-related losses that occur during a switching cycle.

Gate charge (Q_G), is the total amount of charge required to turn on the device, shown in Figure 1.8. For the GaN device, Q_G is 40 times lower than the Si device, resulting in lower gate drive losses. Another benefit of lower gate drive loss is a reduction in power required by an auxiliary power supply, which often occupies notable board space and has non-negligible power loss.

Gate-to-drain charge (Q_{GD}), often referred to as Miller charge, is the amount of charge during voltage commutation, shown in Figure 1.8. For the GaN device, Q_{GD} is 30 times lower than the Si device, resulting in lower voltage commutation losses.

Gate-to-source charge (Q_{GS}), is the amount of charge needed to reach the device's threshold voltage (Q_{GS1}) and rise to the Miller plateau voltage (Q_{GS2}), shown in Figure 1.8. For the GaN device, Q_{GS} is 35 times lower than the Si device, resulting in lower current commutation losses, which occur in the Q_{GS2} timing of Figure 1.8.

Output capacitance (C_{OSS}), is the sum of drain-to-source and gate-to-drain capacitance. Output capacitance must be discharged or soft-commutated during each switching cycle. For the GaN device, C_{OSS} is 3 to 10 times lower than the Si device, respectively for high (50 V) and low (1 V) blocking voltages. In hard-switching applications, output capacitance loss is related to V_{DS2} and the higher blocking voltage output capacitance condition is of more importance. In soft-switching applications, where soft-switching is generally achieved in relation to V_{DS}, the larger output capacitance value, which occurs at lower blocking voltages is of more importance. Regardless of the design topology, the GaN device has lower C_{OSS} related losses.

Reverse recovery (Q_{RR}), is the stored charge in the body diode of a MOSFET that must be discharged before the MOSFET can block voltage and is a major source of loss in a synchronous rectifier (SR). For the GaN device, which has no minority carriers and zero Q_{RR}, reverse recovery losses are infinitely lower than the Si device.

Source-to-drain forward voltage (V_{SD}), also known as body diode forward voltage in MOSFETs, is the conduction voltage when a synchronous rectifier device is off and must conduct current for generally a short dead time before the control device is commanded on as shown in Figure 1.8. For the GaN device, the forward conduction losses are 1.5 times higher than a Si device. More than offsetting this higher loss component, GaN has significantly lower charges/capacitances and associated losses compared to a Si MOSFET.

For the design shown in Figure 1.9, the GaN power semiconductor losses are reduced by a large enough factor that, at only 1/10th the size of a Si MOSFET, the GaN device is still not the thermal bottleneck of the system. This achievement is not possible without a superior GaN power semiconductor.

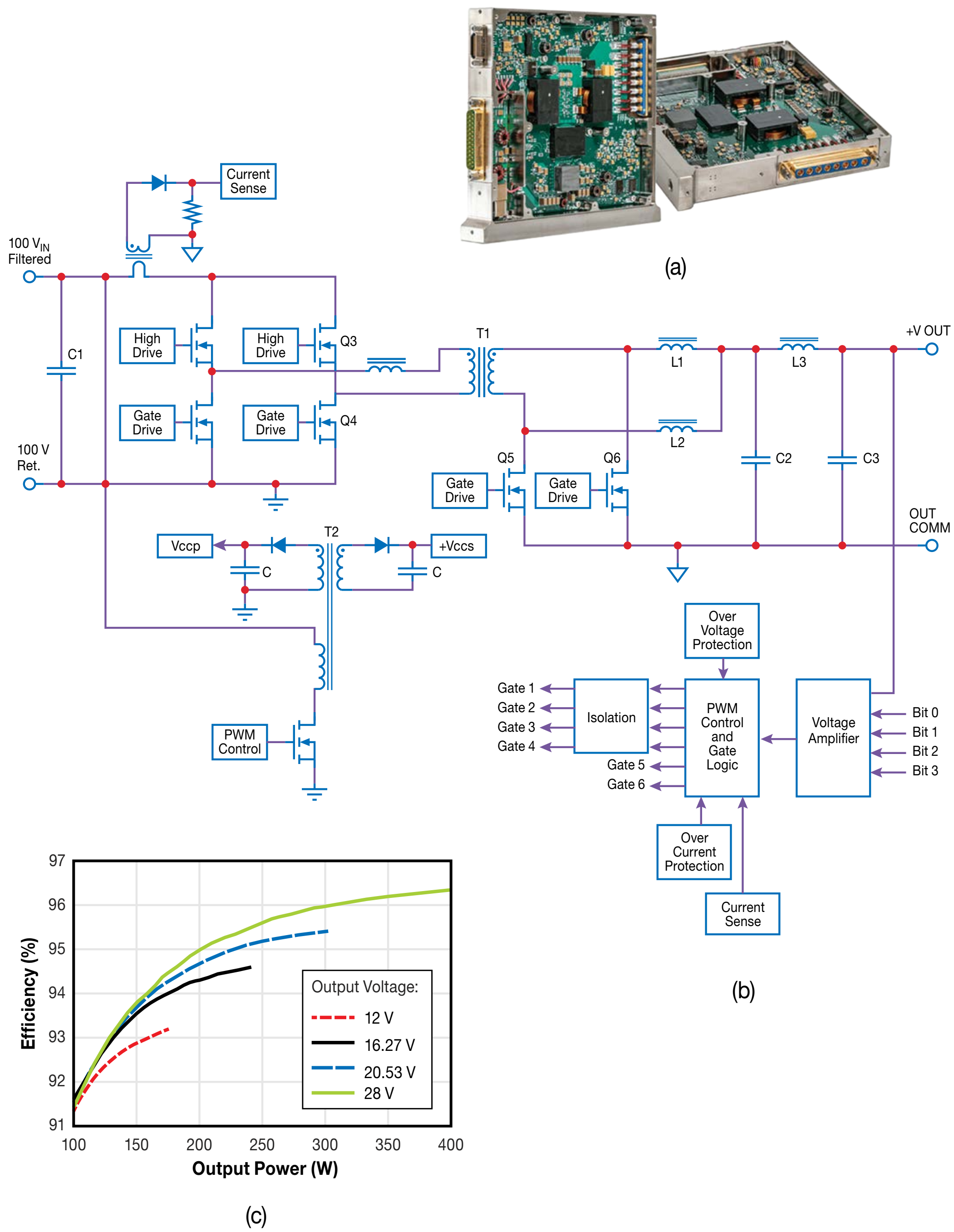


Figure 1.9 VPT SGRB10028S DC-DC converter (a) hardware, (b) topology, and (c) V_{IN} = 100 V efficiency

Combining advanced GaN power semiconductors and state-of-the-art design techniques enables a new level of performance in high reliability space designs as demonstrated in Figure 1.9. The VPT SGRB series have been designed specifically for space-borne telecommunications where high efficiency, low noise, and radiation tolerance are imperative. Using advanced GaN-based technology, the SGRB series was developed to provide a solution that increases power supply efficiency, while reducing system size, weight, and cost. In the next section, GaN power devices used in motor drives designed for space are discussed.

1.3 Motors and Motor Driver Applications in Space

Applications requiring motion systems in space must deal with environmental issues not found in motion systems used in terrestrial systems. The challenges in space also vary according to the physical location of the system, particularly with regard to radiation. For example, satellites in Earth's orbit must deal with radiation fields not found in stationary locations such as those on the surfaces of the Moon or Mars.

The type and magnitude of radiation encountered in Earth's orbit is also greatly influenced by the orbital altitude of the satellite. Satellites in low Earth orbit (LEO) have a different radiation-hardness requirement than those in geosynchronous Earth orbit (GEO) satellites. Landers and missions to the Moon and other planets have another set of radiation requirements that they must tolerate. Finally, deep space probes have yet another set of radiation requirements. The radiation profile over the life of the satellite or spacecraft must be determined and specified, and the proper components for each piece of the motion control system carefully chosen if the desired lifespan for the system is to be achieved.

For a motion control system, the weakest link in the system in terms of radiation susceptibility are the electronics associated with the motor drivers. The motors themselves present a very robust component of the system – from an electrical perspective they are constructed from wire and thus present an inherent radiation hardness during their operation in space. This is not true of the electronics that make up the motor driver. There are numerous interconnected semiconductor components in a motor driver, from the power switches for the motor windings to the associated catch diodes to the electronics that interface between the circuity that generates the PWM or dive command signals for the power switches and the power switches to the PWM circuitry itself. All these circuits and their constituent components must have an assured, that is a tested level of radiation hardness for the mission to succeed long-term.

GaN products intentionally produced for use in satellites consist of discrete GaN transistors as well as more complex circuit functions incorporating these devices. The discrete devices are available as hermetically-sealed devices in thermally-efficient aluminum nitride ceramic packages and wafer level chip-scale packaging (WLCSP) for hybrid applications. The modular devices have electrical functions that range from: single and dual low-side gate drivers; to single and dual low-side power drivers, which incorporate GaN-driving-GaN gate drivers along with GaN transistor switching elements and Schottky catch rectifiers; to a half-bridge driver as part of independent low- and high-side power drivers.

For example, the EPC Space FBS-GAM02-P-R50 [12] module can be readily configured in a half-bridge configuration as shown in Figure 1.10. This module is housed in an 18 pin, non-hermetic plastic over-molded package. In addition to the power half-bridge function with low- and high-side switches and gate drivers, this module also incorporates the high-side bootstrap capacitor and diode, an under-voltage "power good" function and input shoot-through protection (to prevent the power switches from being activated/turned ON simultaneously). With V_{DD} connected to the desired motor voltage (V_{motor}), T_{OUT} and B_{OUT} connected as the switching node, V_{BIAS} (the gate driver supply voltage set to 5 V_{DC}), and PGND connected to ground (0 V_{DC}) the GAM02 module serves as a 50 V, 10 A half-bridge power driver. The higher level of functional integration offered by this device allows digital PWM signals at the B_{IN} and T_{IN} logic inputs to directly control the state of the T_{OUT} (high-side) and B_{OUT} (low-side) power switches in the module.

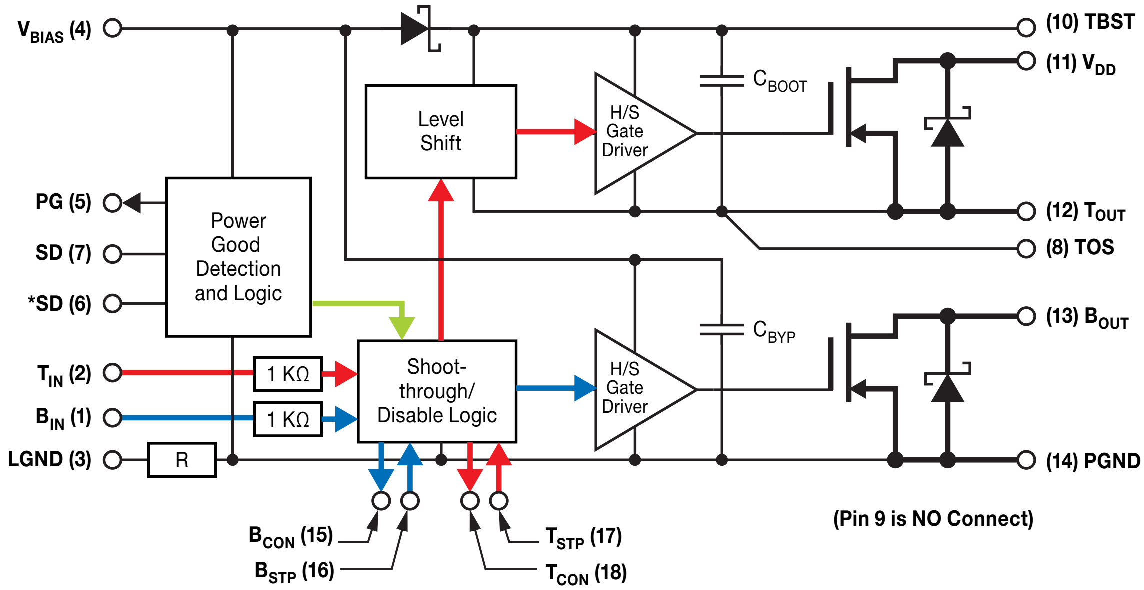


Figure 1.10 EPC Space FBS-GAM02-P-R50 functional block diagram

The GAM02 module allows the designer the ability to provision a low parts-count motor driver solution that is inherently radiation hard for motors requiring bipolar drive. Discrete GaN transistors combined with gate driver modules make it possible to efficiently drive motors to 300 V and to more than 30 A if multiple transistors are paralleled. Figure 1.11 shows how the FBS-GAM01P-R-PSE [14] allows the configuration of a low- or high-side driver using discrete power elements.

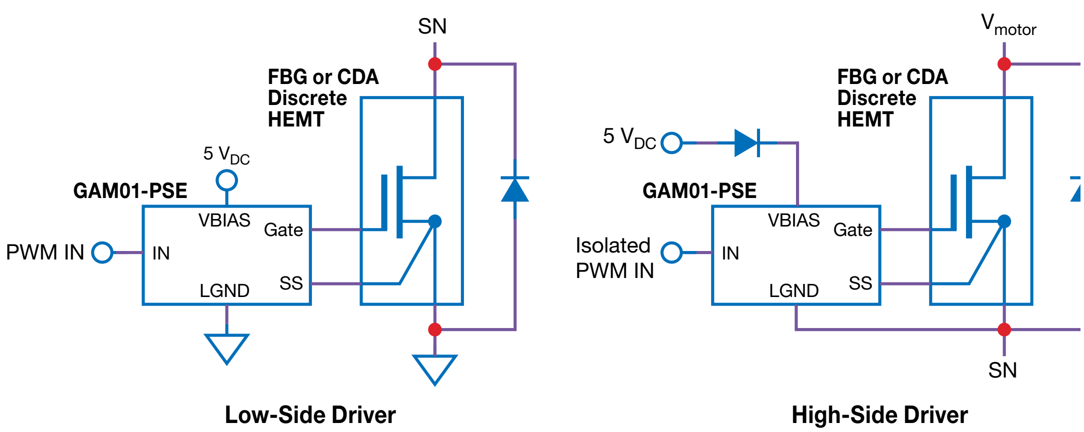


Figure 1.11 EPC Space FBS-GAM01-P-R-PSE as low- or high-side driver

The EPC7C006 [15] demo board is designed to be either stand-alone, the phases driven by external PWM signals, or to interface with the EPC9147A [13] microcontroller interface board featuring a Microchip DSP to provide the PWM signals for each phase based on voltage, current and optional positional feedback. This control board utilizes the Microchip motorBench® development suite. Thus, the designer has the means to control the motor to be driven in the end-application with an existing control system developed in-house or with a purpose-built control system that interfaces to a computer via a USB connection and GUI interface.

The EPC7C006 board, which measures 6.50 x 5.22 inches, is shown in Figure 1.12. In addition to three-phase motors, multiple EPC7C006 boards may be used to drive multiphase stepper motors or multiple single-phase motors. So long as the appropriate PWM signals are available, there is no limit to the applications that this flexible demo board can satisfy.

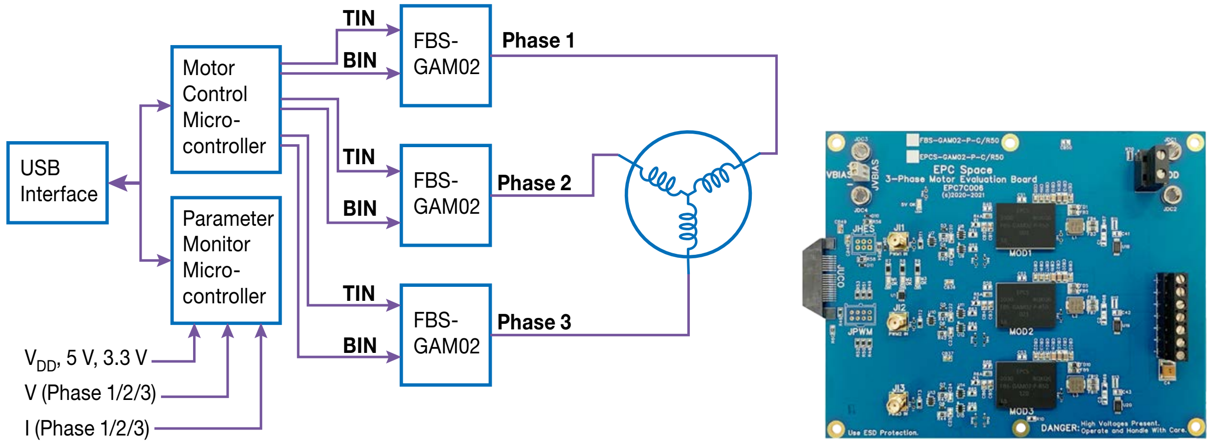


Figure 1.12 EPC Space EPC7C006 three-phase motor driver board and block diagram

1.4 Rad-Hard Integrated Circuits

eGaN power devices use a lateral conduction structure between drain and source terminals with the current modulated by the gate terminal. The construction of the device relies on multiple metal layers acting as interconnects to connect the thousands of unit cells in parallel to form the single power device. Alternatively, each lateral GaN unit cell can be scaled to different voltages, currents, switching speeds and parametric matching requirements as needed by circuit design. Then the different devices can be interconnected into an integrated circuit (IC) with additional device elements such as integrated resistor and capacitor as discussed in Chapter 1 of our text book ***GaN Power Devices and Applications***.

One inherent advantageous attribute of the GaN IC structure is the built-in radiation hardness of all its integrated devices. All the radiation-hardness properties of the GaN devices, as described earlier in the chapter, are still present in their integrated forms. Understanding the radiation effects allow circuit designers to design circuits and products that have superior radiation-hardness specifications compared to Si integrated circuits.

Using gallium nitride IC technology, circuit designers gain greatly increased integration density for size reduction and can also benefit from the inherent advantages of the higher performance levels of monolithic integration not easily achieved with discrete or hybrid implementation.

One such example is the integrated half-bridge power stage IC as shown in block diagram form in Figure 1.13 and discussed in detail in Chapter 1 of EPC's latest text book, ***GaN Power Devices and Applications***.

This monolithic IC includes the output high-side and low-side eGaN power devices configured as half bridges, the floating high-side gate driver, the fixed referenced low-side gate driver, the level-shifting circuits, the synchronous bootstrap circuit and the input logic circuit [16].

In addition to the dramatic reduction in size of the monolithic integrated half-bridge IC as compared to hybrid integration, inherent IC device matching advantages give circuit designers the flexibility to design more advanced analog circuits. Examples of such circuits incorporated into the integrated half bridge IC are easy interfaced to an MCU, gate drive and bootstrap supply management, delay matching and deadtime management, output FET switching time tuning to optimize efficiency vs. over-voltage spike, fault conditions lockout logic [17] and could even extend to RC oscillator, PWM modulator and feedback control loop circuits.

Because the GaN power devices are on the same chip with the control circuit, on-chip sensing of the output switching node transient voltage can help to facilitate closed-loop adaptive dead-time control, automatic detection of negative transient conduction and activation of synchronous rectification mode, which is especially important for GaN output power stage with its higher negative clamp voltage than the Si MOSFET anti-parallel diode. Other on-chip sensing techniques with $R_{DS(on)}$ sensing, low resistance current sensor or linear temperature sensor helps to implement over-current and over-temperature fault detection and safe shutdown [18].

The function of a simple gate driver is very useful for higher current applications when GaN IC monolithic integration of control and GaN output devices would result in too large a die size. Gate drivers designed to drive discrete enhancement-mode GaN devices are readily available in the commercial market. These Si-based gate-driver ICs are implemented in CMOS or BiCMOS technologies. Radiation-hardened versions of the gate-driver ICs are available [19] but not very common, and very expensive. In addition, the electrical and radiation-hardness specifications need to be improved to meet ever more stringent requirements for the applications as shown in the real-world product example of the VPT SGRB10028S DC-DC converter (see Section 1.3) that uses at least six radiation hardened gate-driver ICs.

An obvious application for the GaN IC technology would be to implement gate-driver ICs that take advantage of the inherent radiation-hardness properties of the GaN IC technology. It is tempting to think that it is a simple cut and paste to implement the gate-driver IC from the integrated half-bridge IC, however, the parasitic elements of driving external GaN transistors must be carefully considered.

In Chapter 2 of our text book ***GaN Power Devices and Applications***, Figure 2.13 shows the various parasitic inductances in the gate drive loop, as well as in the power loop. Figure 1.13 is a block diagram of a half-bridge gate driver IC implemented in GaN IC technology. Besides superior radiation-hardness specifications, important elements in the GaN IC implementation include regulated gate drive voltage tailored to drive external GaN transistors, synchronous bootstrap charging using an internal GaN transistor, robust high side and low-side level shifting without false trigger from fast transients and over-voltage spikes caused by the external eGaN output transistor switching and separate pull-up and pull-down path for the gate-drive loop to tune the switching time to minimize effect of common source and power loop inductances.

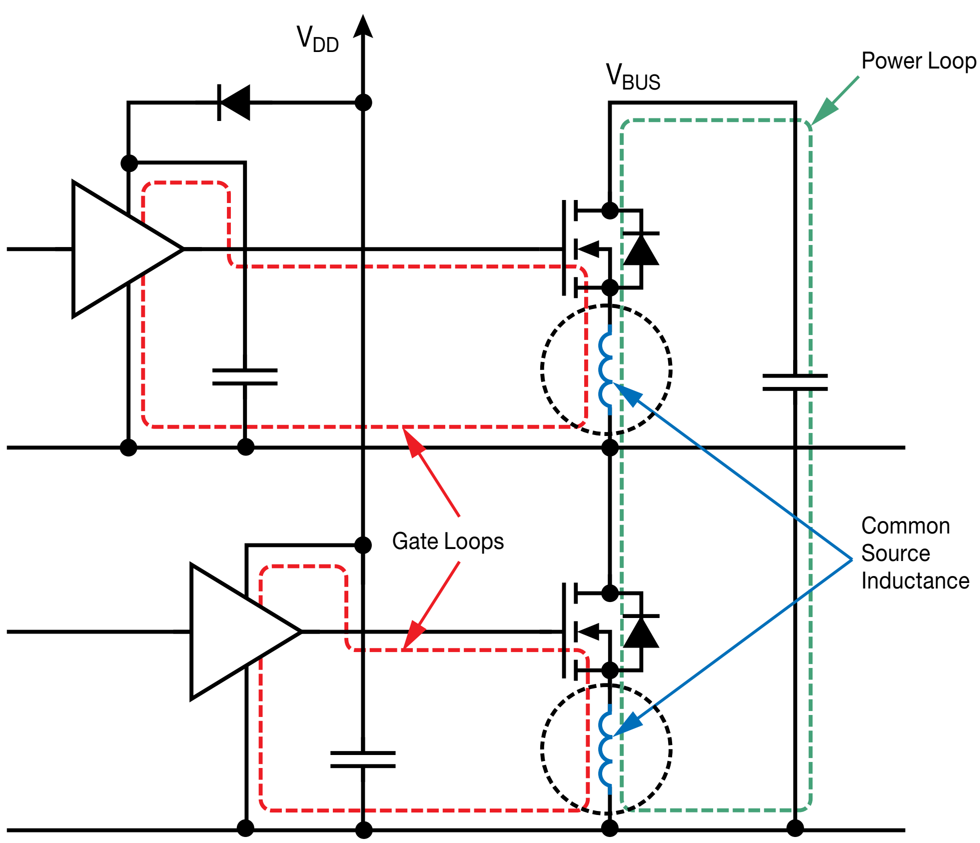


Figure 1.14 .Schematic of a half-bridge power stage showing power and gate drive loops with common source inductance shown in dotted circles

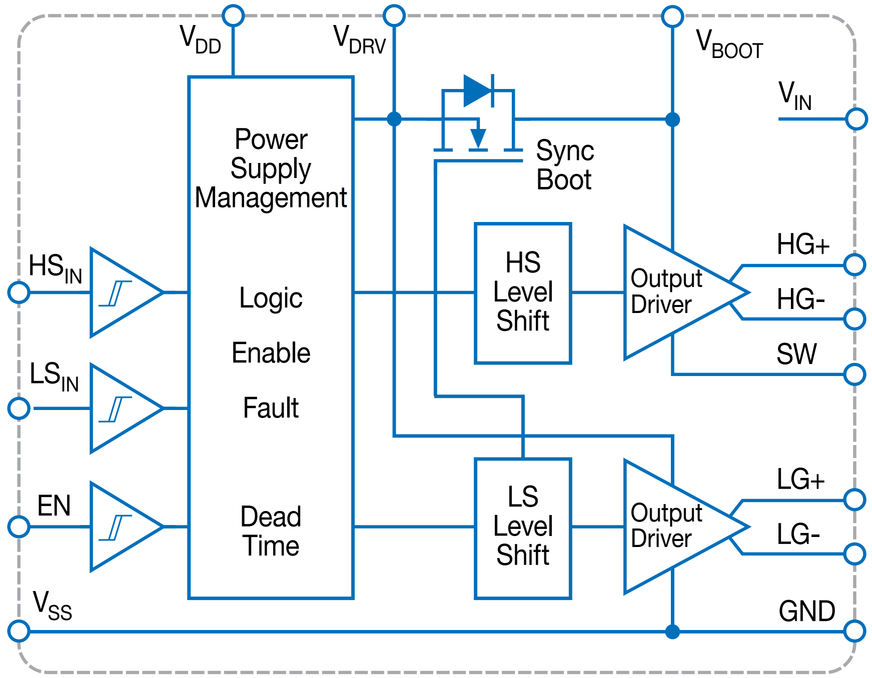


Figure 1.13 Half-bridge gate driver IC block diagram

CERN, the world's largest particle physics research laboratory, and EPC are engaged in a collaborative project to demonstrate the effectiveness of a radiation-hardened controller IC from CERN working as a chipset with the EPC integrated half-bridge power stage IC. The end application is a 48–12 V, 10 A buck converter operating at 1–3 Mhz. A custom 80 V controller IC is designed by CERN. The chip uses an 80 V Si BiCMOS technology with device, circuits, and layout techniques specifically designed for radiation hardness. Several generations of the controller and power stage ICs have been designed and are in production [20].

The goal of the new chipset is to use a 48 V input to reduce current flow, and thus weight and size, of the power distribution harness. All the ICs in the chipset must tolerate the magnetic and radiation environment within the Large Hadron Collider (LHC) and the radiation specifications operating in the space environment.

Figure 1.14 is a block diagram and photo of the actual PCB of the two ICs working together to form the control loop and power paths for the 48 V–12 V DC-DC converter. The control loop is internally compensated and the PWM modulator is optimized for 1–3 MHz switching to minimize the size of the output inductor. Bias power for the GaN power stage is generated and regulated from the controller IC. An innovative predictive dead-time circuit is used to adaptively adjust the timing to achieve optimal dead time for the power stage. Electrical performance of the DC-DC converter is superior to any previous radiation-hardened solutions with peak efficiency over 96% at 10 A load current with 1 MHz switching as shown in Figure 1.15.

The 48 V_{IN} DC-DC converter with a 235 nH air core inductor has been irradiated with x-rays to study the Total Ionizing Dose (TID) effects. The X-ray irradiation system is the Seifert RP149 that is routinely used for TID tests of deep sub-micron technologies. With a 50 kV, 3 kW tube, a tungsten target, and a 150 μm Al filter, the system produces an X-ray spectrum that has been well characterized in literature and is well accepted by the radiation effects community.

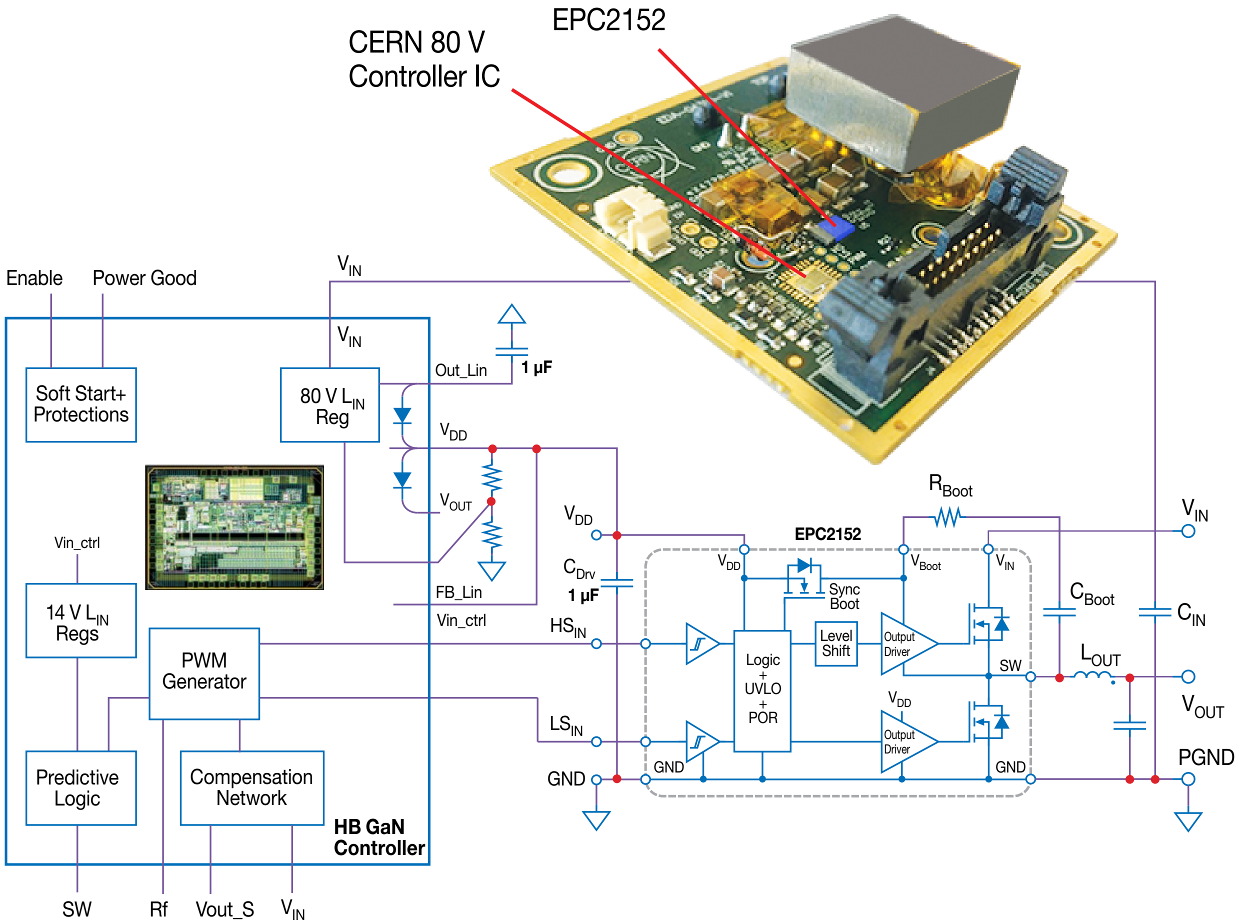


Figure1.14 CERN/EPC chipset for 48 V_{IN} to 12 V_{OUT} DC-DC Converter.

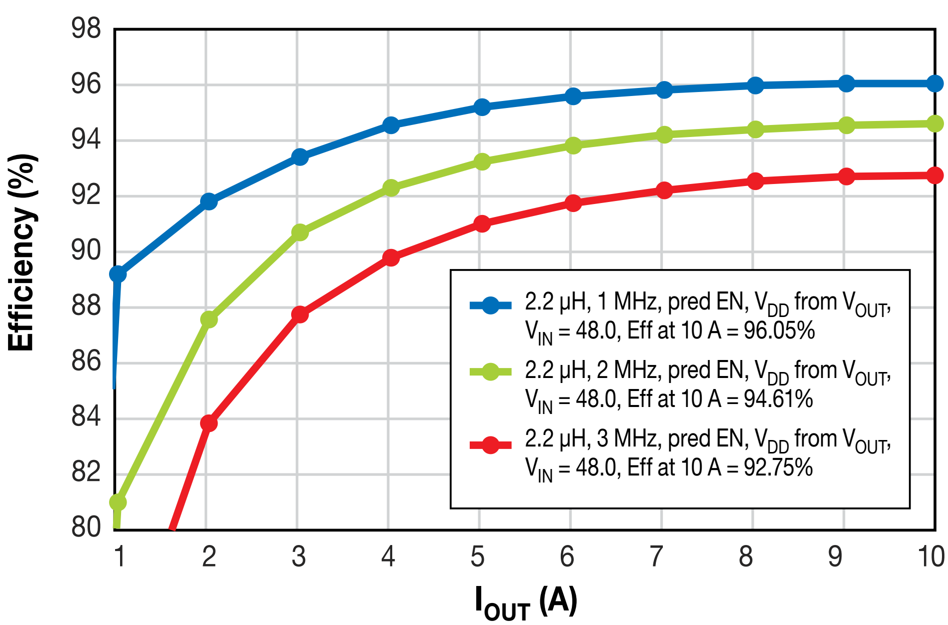


Figure 1.15 Performance of the CERN/EPC chipset for 48–12 V buck converter operating from 1–3 MHz

Figure 1.16 and Figure 1.17 show the V_{OUT} and efficiency vs. TID, respectively. Both plots have two x-axes because the deposited dose differs with material – the controller IC is in Si, and the power stage IC is in GaN. The variation with TID is minimal up to a TID of 50 MRad for the Si controller IC and 100 MRad for the GaN power stage IC.

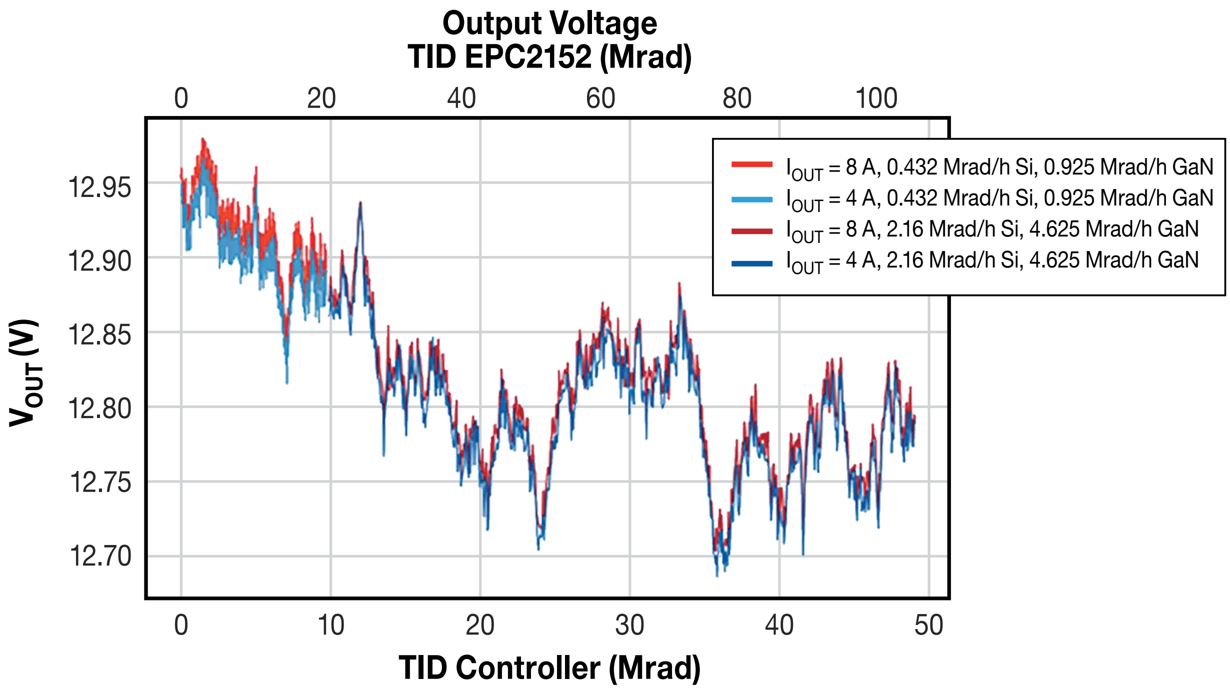


Figure 1.16 Output Voltage vs. TID for Controller IC and for power stage IC

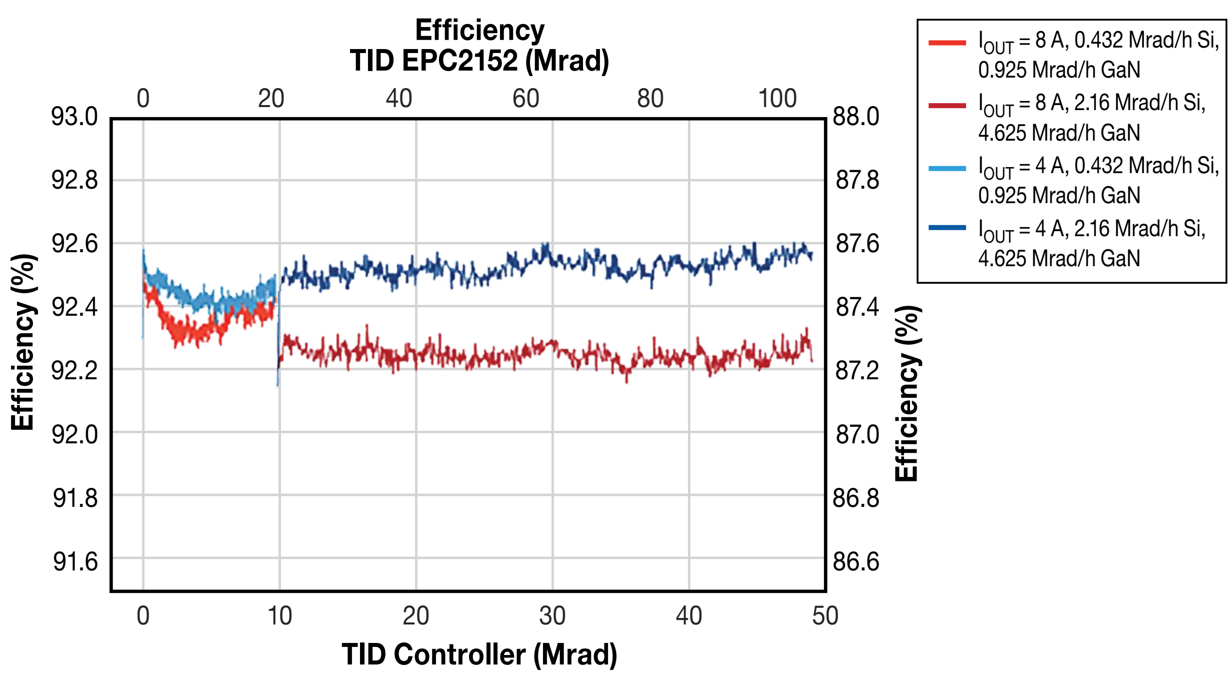


Figure 1.17 Efficiency vs. TID for controller IC and power stage IC

A SEE test has been performed in the Cyclotron Resource Center of UCLouvain specifically for ions hitting the surface of the exposed controller IC inside a DC-DC converter using the chipset. Ni and Rh ions are used to achieve LET level from 28.8 to 40.8 MeV·cm²/mg with the results shown in Figure 1.18. The V_{OUT} event's amplitude, waveform and histogram are recorded. Variations are within the 10% tolerance, and no device failures were recorded. An improvement to the controller IC will enable LET performance levels up to 80 MeV·cm²/mg for the space application specifications.

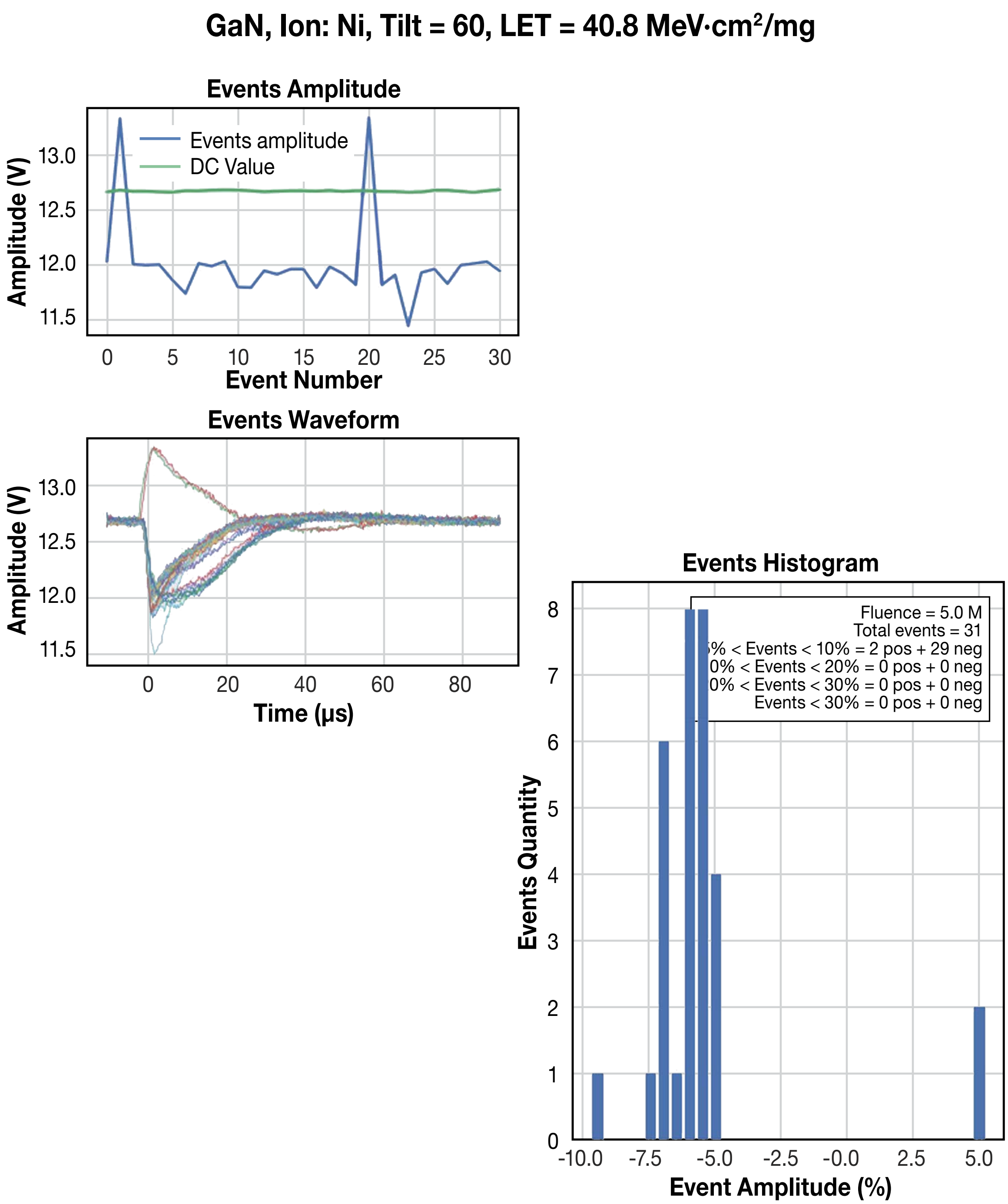


Figure 1.18 DC-DC converter V_{OUT} event's amplitude, waveform, and histogram under single event effects test for the controller IC

The EPC2152 [17] Integrated ePower™ Stage was tested individually at the Texas A&M Cyclotron Radiation Effects Facility (TAMU) to evaluate its vulnerability to Single Event Effect. The EPC2152 was tested in a buck converter configuration as shown in Figure 1.19 with a 12 V input and operating at 200 kHz while the output voltage switching node was monitored.

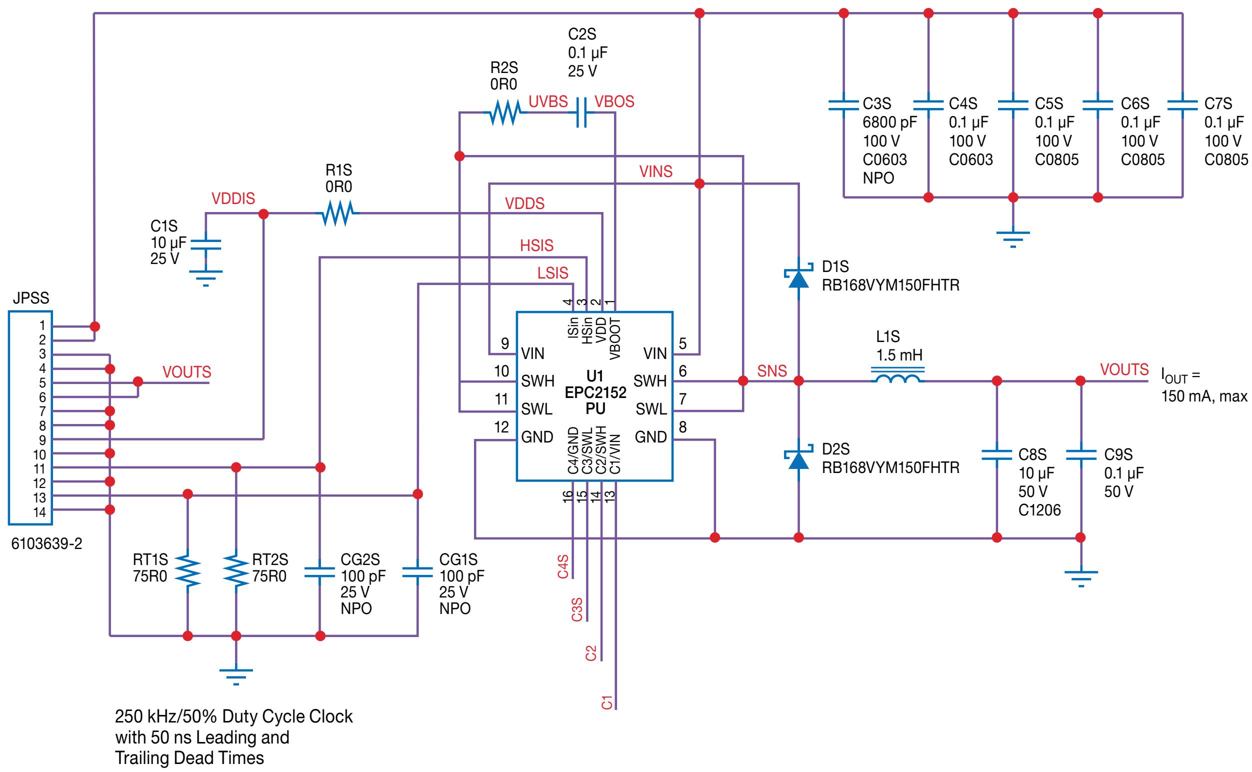


Figure 1.19 Single event in situ test circuit for the EPC2152

The SEE testing was perform at 25°C and at normal incidence for the worst-case condition as demonstrated on discrete GaN transistors. LET levels of 56 and 83 MeV·cm²/mg were used with a minimum ion penetration range of 100 µm.

The EPC2152 was found to be immune to SEE with no degradation to the switching output node up to 50 V with a LET of 83.3 MeV·cm²/mg. Table 1.4 summarizes the beam conditions and recorded events. The three events recorded on sample 3 with a LET level at 56.1 MeV·cm²/mg were not destructive nor showed any SEU output upsets. Figure 1.20 shows the envelop tracking set to detect any events in the switch output node voltage greater than to plus or minus −0.25 V during a run with a LET of 83.3 MeV·cm²/mg.

Sample	LET (Si) MeV·cm²/mg	Energy MeV	Range µm	Flux MeV·cm²· sec	Fluence #/cm²	Angle Deg	V_{DD} (V)	VSW	# events
1				1.05E+04					0
2	56.1	1473	108.1	1.06E+04	1.00E+07	0	12	40	0
3				1.20E+04					3
1				1.02E+04					0
2	83.3	2256	121.4	1.13E+04	1.00E+07	0	12	40	0
3				1.16E+04					0

Table 1.4 Summarizes the number of events and beam conditions during SEE for the EPC2152

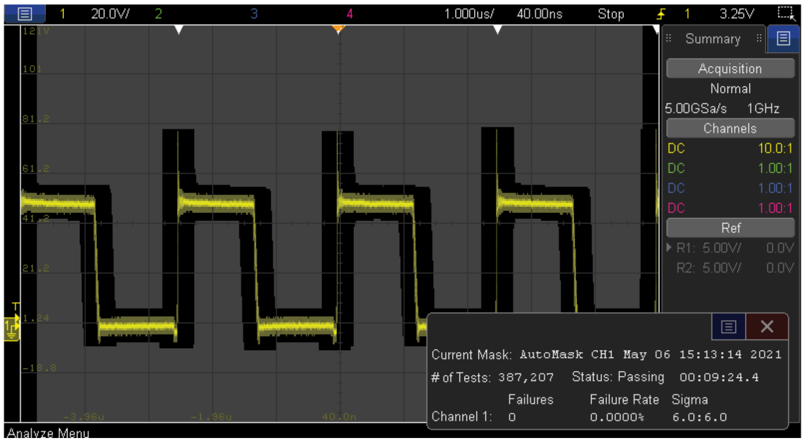


Figure 1.20 EPC2152 switching output node at LET = 83.3 MeV·cm^2/mg

2.0 Summary

Space is a challenging environment for semiconductor components. Constraints such as size and weight are coupled with the need for a high tolerance of various forms of radiation. Solutions in silicon have been available for many years but required compromise in size and weight due to reduced electrical performance and the requirements for various amount of shielding from harmful radiation. GaN transistors, hybrid circuits, and integrated circuits create more than an order of magnitude improvement in electrical performance as well as radiation resistance. This opens up new opportunities to improve existing systems and potentially to change power architectures that further improve efficiency, size and weight.

For more information regarding EPC's rad-hard packaged solutions visit **epc.space**. For rad-hard wafer level chip-scale package solutions and additional design support visit **epc-co.com**.

Additional information describing GaN technology, attributes, design tips and reliability in available in EPC's latest textbook ***GaN Power Devices and Applications.***

For design assistance submit a request to Ask a GaN Expert

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